

JUN 12 2007

Application No.: 10/823,489

Docket No.: JCLA12709

**In The Specification:**

Please amend the paragraph [0061] as follows:

[0061] Refer to Fig. 11, which illustrates a scheme of the time delay synchronous control for the post buck converter 902. The buck switch  $Q_1$  begins to turn on ~~synchronously with the rectifier diode  $D_1$~~  at time  $t_1$  when the flyback converter has a pulse current to the output capacitor and turn off at time  $t_2$  before the time of  $t_3$  when the main switch  $S_1$  of the flyback converter 901 turns on. Thus, as Fig. 11 shows, a final ripple current  $i_{cf1}$  on the output capacitor  $C_{f1}$  is achieved with a significantly reduced *rms* value compared with the original  $i_{cf1}$  without the post buck converter.